ABSTRACT OF THE DISCLOSURE

A memory device and fabricating method thereof. In the memory device of the present invention, a substrate has a plurality of deep trenches, wherein the deep trenches formed in the adjacent rows are staggered. A deep trench capacitor and a control gate are disposed in each deep trench successively. Word lines are disposed on the control gates respectively, and each word line is electrically coupled to the control gate thereunder. Diffusion regions are disposed in the substrate and surrounding the deep trenches respectively to serve as sources of vertical transistors. Each diffusion region is electrically connected to the surrounding deep trench capacitor. Active areas are disposed on the rows of the control gates respectively along a second direction. The regions where each active area overlaps the control gates have at least one indentation.